**The University of the West Indies**

**Department of Computing and Information Technology**

**COMP 2601 – Computer Architecture**

**Assignment 1**

**Date Given**: 8th October

**Date Due:** 28th October

**Instructions:**

This is an Individual assignment, therefore all work submitted must be your own. Please name your file using your ID number and course code. Submission is via a Turnitin link on myElearning.

1. Given the following truth table,
   1. write the SOP form of F [1 mark]
   2. use Boolean Algebra to reduce the expression in a. [3 marks]
   3. draw the Karnaugh map for the expression in a., showing groupings, and giving the simplified expression obtained [3 marks]
   4. draw the circuit for the simplified expression. [1 mark]

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | D | F |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

* 1. Use Booth’s algorithm to multiply 31 (Multiplicand) by 29 (Multiplier), where each number is represented using 6 bits. Working for all cycles of the algorithm must be shown. Use the following table: [4 marks]

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **A** | **Q** | **Q-1** | **M** | **Steps** | **Cycle** |
|  |  |  |  |  |  |

* 1. Do you get the same answer if the Multiplicand is 29 and the Multiplier is 31 (M and Q are interchanged) and the same algorithm is followed? [1 mark]

1. Write generic instructions to compute F = r – ((tq + s) + t/r) using a processor that supports:
2. 3-address instructions, using 3 registers [3 marks]
3. 2-address instructions, using 2 registers [3 marks]
4. 1-address instructions, using the accumulator [3 marks]
5. a zero-address instruction on a stack-based processor. [2 marks]

You may assume operations in the following table where R1, R2, R3 are registers and A is a memory address.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **3-address** | **meaning** | **2-address** | **meaning** | **1-address** | **0-address** |
| ADD R1, R2, R3 | R1 ← R2 + R3 | ADD R1, R2 | R1 ← R1 + R2 | ADD A | PUSH A |
| SUB R1, R2, R3 | R1 ← R2 - R3 | SUB R1, R2 | R1 ← R1 - R2 | SUB A | POP A |
| MUL R1, R2, R3 | R1 ← R2 \* R3 | MUL R1, R2 | R1 ← R1 \* R2 | MUL A | ADD |
| DIV R1, R2, R3 | R1 ← R2 / R3 | DIV R1, R2 | R1 ← R1 / R2 | DIV A | MUL |
| LOAD R1, A | R1 ← A | LOAD R1, A | R1 ← A | LOAD A | DIV |
| STORE A, R1 | A ← R1 | STORE A, R1 | A ← R1 | STORE A | SUB |

1. Refer to the Machine Architecture described at the end of this assignment sheet for this question.

Suppose the following program is stored in main memory beginning at address 40 (hexadecimal). Also suppose memory address 00 contains 05, memory address 02 contains 0A, and memory address 04 contains 0F.

Describe the tasks performed when it is executed.

What is stored at memory addresses 11, 13, and 15 (hexadecimal)?

What pseudocode can you decipher, that the program is performing?

Show your steps in decoding the instructions in the program. [17 marks]

2006

2102

2200

2311

1500

3511

5221

5331

3249

334B

B258

B048

C000

1. Convert the following into MIPS code: [8 marks]

main() {

int x = 10;

int y = 15;

int z;

if(x > 5) {

z = product(x, y);

x = x + z;

}

else {

z = product(x, y);

y = y + z;

}

}

int product(int a, int b) {

return a \* b;

}

1. Assume processor registers PC, MAR, MBR, IR, a base register **BA**, a data register **R1**, and that **A** is a decimal value. List the sequence of micro-operations performed on these registers during the execution of each of the following:
   1. Interrupt cycle [4 marks]
   2. LOAD R1, A (immediate addressing) [2 marks]
   3. SUB R1, R1, A (indirect addressing) [3 marks]
   4. Branch A (PC relative addressing [2 marks]
   5. Branch A (displacement addressing) [2 marks]
2. Research the following:
   1. Describe and contrast the two methods of byte ordering: big-endian and little-endian. [4 marks]
   2. Since there is no consensus on which byte ordering style is superior, state 2 points in favour of each method. [4 marks]

You may refer to Appendix 12A of your text for information.

**[Total = 70 marks]**

**Please refer to the following Machine Architecture description and instruction set in this page and the next, for question 4 above.**

Text, letter

Description automatically generated

A screenshot of a computer

Description automatically generated with low confidence